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12TH MICRO/NANO-ELECTRONICS PACKAGING AND ASSEMBLY, DESIGN AND MANUFACTURING FORUM

MiNaPAD Forum 2026

June 3th - 4th
Minatec
Grenoble - France

- ▶ Exhibitions
- ▶ Conferences



Organized by IMAPS France - International Microelectronics Assembly and Packaging Society
17 rue de l'Amiral Hamelin - 75016 Paris - France

Wednesday June 3th



8h30 Registration and Welcome to MiNaPAD – Coffee & Soft drink sponsored by
9h00 Opening by Valérie VOLANT (Auditorium)

9h10 Keynote 1 : **Corinne Crégut and Emmanuelle Serret, R&D directors, STMicroelectronics, France**
IDM End-to-End Co-Optimization of Front-End and Back-End for Robust, Cost-Effective Microelectronics Products

SESSION A: Dispensing technologies (Auditorium)

10h00 Real-Time Inline Monitoring of Adhesive Mixing for Process Control in Electronics Packaging
([R.A. Acedera](#), Krayden, Philippines)

10h30 Advances in Sintering Materials for Varying Substrate Sizes "From Slit-Nozzle Dispensing for large substrate area to Jet Dispensing for small diodes
([A.M. Laügt](#), Inventec, France)

SESSION B: Attachment materials (Chrome)

Development of an electrically conductive, B-stageable adhesive for reliable ceramic MEMS package assembly
([J. Schuermans](#), Roartis, Belgium)

AI Data Centre ASIC Cooling – Advanced Solder-TIMs
([K. Vijay](#), Indium Corporation, United Kingdom)

11h00 – 11h30 Exhibition Opening (Exhibition Hall) / Coffee break sponsored by



SESSION C: Sustainability (Auditorium)

11h30 Additive manufacturing fabrication and LCA of PCBs for remote control
([T. JAMAL](#), CEA Liten, France and [E. WHITMORE](#), 4MOD Technology, France)

12h00 Learn about 3D integration through its environmental impact
([M. Billaud](#), CEA Leti, France)

SESSION D: Sintering materials (Chrome)

Pressure-less silver sintering for power application: impact of silver, gold or copper surface finishes on microstructure and mechanical performances
([M. Veluire](#), UGA / CEA Leti, France)

Evaluation of various Cu-sinter materials using different sintering atmospheres and conditions
([S. Merkert](#), PINK GmbH Thermosysteme, Germany)

12h30 – 13h40 Lunch (Exhibition Hall) sponsored by



13h40 Keynote 2 : **Steffen Kröhnert, President & Founder, ESPAT-Consulting, Germany**
Electronics Packaging in Europe - Where we are three years after EU Chips Act 1.0

SESSION E: Packaging Architecture (Auditorium)

14h15 Low Profile Waterproof Pressure Sensor
([A. Ratti](#), STMicroelectronics, Italy)

14h45 Case studies: applied reliability for European electronics
([M. Wallrodt](#), Micro Systems Engineering GmbH, Germany)


15h15 Toward a reproducible fabrication process of a magneto-optic trap for ultra-cold atom sources.
([L. Boudier](#), Univ de Toulouse /LAAS-CNRS, France)

SESSION F: Reliability (Chrome)

Platform for the characterization of electronic components during aging under thermal and electrical stresses
([C. Rouleau](#), Univ de Bordeaux / EDF, France)

Thermal Cycling Durability Model for Lead-Free Wafer Level Packages
([J-B Libot](#), [P. Milesi](#), Hooke Electronics, France)

Sinter Lamination in Planar Transformer PCB Technology: Reliability Assessment and Path Towards ECSS Standardization for Aerospace Applications
([I. Platteaux](#), Advanced Circuit Boards (ACB), Belgium)

15h45 – 16h15 Exhibition / Coffee break sponsored by 

**SESSION G: Process optimization
(Auditorium)**

16h15 Optimizing indium bump deoxidation through 3D surface profilometry
[\(G. Chaumy, A. Griffart SET Corporation, France\)](#)

16h45 Atmospheric Plasma Processes for Sustainable Oxide Reduction and Adhesion Enhancement in Power Electronics Packaging
[\(D. Ben Salem, Plasmatrete GmbH, Steinhagen, Germany\)](#)

17h15 Enhancement of Gold-to-Gold (Au-Au) Bonding by atmospheric plasma surface treatment
[\(D. Pascual, ONTOS Equipment Systems, USA\)](#)

**SESSION H: Characterization
(Chrome)**

Warping control during assembly process and panel-level RDL formation for heterogeneous integration
[\(Y. Maruyama, Resonac Corporation, Japan\)](#)

Synchrotron X-ray microtomography, an advanced imaging technique to reveal electronic devices packaging and assembly.
[\(E. Boller, F. Léonard, B. Feit, P. Gravie The European Synchrotron, Insidix, France\)](#)

Multi-scale micromechanical testing for new Polymer Core Solder Ball interconnection's reliability in operating conditions
[\(Y. Marthouret, X. Carridroit, EMSE, Thales AVS, France\)](#)

17h45 - 18h30 Exhibition Hall

17h50 - 18h10 **Extra session (Auditorium)**
PEPR Packaging (INPACK) and ReNaPack - Projects overview
[\(O. Ducloux, CEA - D. Henry, CEA Leti - H. Granier, CNRS Laas - France\)](#)
Short presentations of French scope programmes, presented in French only.

18h30 Social Event : Domaine de Charmeil

Bus transportation: meeting point MINATEC (3 parvis Louis Néel 38000 Grenoble)
Departure Time: 18h30

Location: Domaine de Charmeil, 154 Impasse Grande Grange 38210 St Quentin sur Isère
Departure time: 22h30 (Transportation by Bus to Hotel Novotel - 7 Place Robert Schuman 38000 Grenoble)



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Thursday June 4th

8h00 - Opening exhibition and conferences – Coffee & Soft drink sponsored by



8h30 Welcome

8h40 **Keynote 3 : Jérôme Teyseyre, Co-Founder, NexStage.Ventures, Singapore**
Connecting the Dots: From Technical Excellence to Ecosystem Leadership

Session J: 3D advanced (Auditorium)

- 9h15 **Glass 3D structuring via FLICE technology for advanced packaging applications**
([A. Lecomte](#), [D. Bourrier](#), [S. Charlot](#), [B. Reig](#), [V. Bardinal](#), [C. Bernard](#), [P. Pons](#), [H. Garnier](#), Toulouse Univ./ LAAS-CNRS, France)
- 9h45 **Build-Up Fan-Out Wafer-Level Packaging with In-Package Fabrication of 3D Integrated Passive Devices Enabled by 3D- RDL and TPVs for RF/mmWave Applications**
([A. Ghannam](#), 3DiS Technologies, France)

Session K: Advanced packaging (Chrome)

- Aluminium Filled Through Glass Vias (TGV): From Idea to Applications**
([N. Burmeister](#), Fraunhofer Institute for Silicon Technology, Germany)
- New dielectric materials for low temperature hybrid bonding**
([J. Maurice](#), UGA/CEA Leti, France)

10h15 – 10h45 Exhibition & Coffee break (Exhibition Hall) sponsored by



Session L: PCB substrates (Auditorium)

- 10h45 **Substrate Reliability in Practice: Testing Methods and Design Recommendations for IC Packaging**
([D. Capeder](#), Dyconex AG, Switzerland)
- 11h15 **Pioneering Bottom-Up Copper Plating: Advanced Pillar-Like Metallization for High Aspect Ratio Through Glass Vias**
([S. Dharmarathna](#), MacdermidAlpha Electronics Solutions, USA)
- 11h45 **Application of Glass Core Substrates for Chiplet Systems**
([C. Landstorfer](#), [L. Steffen Borchardt](#), [D. Hahn](#), [R. Kahle](#) and [A. Ostmann](#), Fraunhofer IZM, Germany)

Session M: Interconnections (Chrome)

- Innovative Pressureless Wire Bonding for High-Power Systems**
([M. Fettke](#), PacTech - Packaging Technologies GmbH, Germany)
- Ultra-Precise Dispensing for Advanced Microelectronics Packaging: Materials Versatility and Long-Term Process Stability**
([F. Granek](#), [A. Wiatrowska](#), XTPL SA, Poland)
- Investigation of wafer level downscaling challenges in electroplated lead-free microbumps for ultra-fine pitch interconnects**
([S. Grolier-Lee](#), [B. Gauthier](#), [Y. Sahouane](#), [T. Mourrier](#), [C. Pellissier](#), CEA Leti, France)

12h15 – 13h15 Lunch & Exhibition (Exhibition Hall) sponsored by



Session N: Fan-Out (Auditorium)

- 13h15 **Fan Out Wafer Level Packaging – European Manufacturing for Small to Mid-volumes**
([M. Dreissigacker](#), [D. Liesk](#), [T. Braun](#), [M. Wöhrmann](#), [A. Keller](#), AEMtec GmbH, Berlin, Fraunhofer IZM, Berlin, Germany)
- 13h45 **Radar with Integrated Antennas based on Fan-Out Wafer-Level Packaging RDL-First Integration**
([A. Garnier](#), CEA Leti, France)

Session O: Flip-Chip (Chrome)

- Underfill adhesive: Thermomechanical and Thermal Storage Optimization**
([O. N'Diaye](#), PROTAVIC INTERNATIONAL, France)
- Sub-micron placement accuracy – the era for heterogeneous integration and optoelectronic assemblies**
([J. Abdilla](#), [M. Fraubaum](#), [D.C. Sanchez](#), [C. Scanlan](#), BESI Austria GmbH, BESI Switzerland AG)

14h15 – 14h30

Short Break sponsored by



**Session P: Heterogeneous Integration
(Auditorium)**

14h30

Innovative assembly and test developments for next gen power and RF semiconductors
([R. de Wit](#), CITC/TNO, Netherlands)

15h00

Packaging and assembly challenges in Photovoltaic (PV) modules: Focus on numerical simulation of the delamination behavior of PV assembly
([B. Chambion](#), [V. Meslier](#), [J.L. Bouvard](#), [P.O. Bouchard](#), UGA/CEA Liten, Mines de Paris CEMEF, France)

15h30

Innovative Power Package Solutions for AI GPU Accelerators: UTAC's Two-sided Cooling SPS, High Thermal EMC, and SiP Power Module Advancements
([M. Choi](#), UTAC Group, USA)

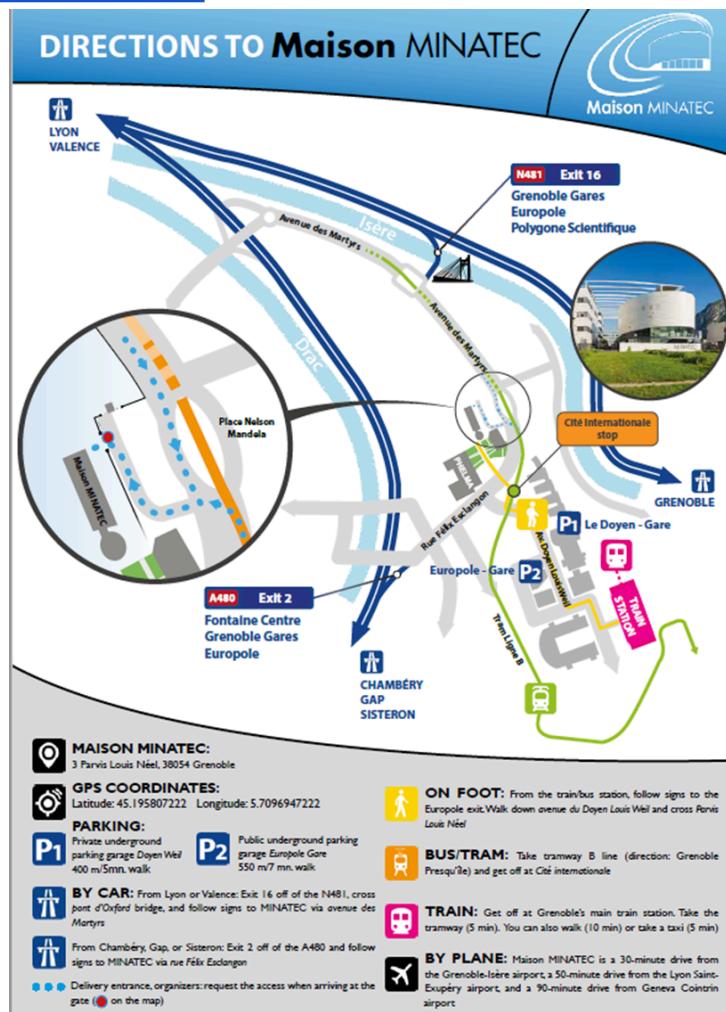
16h00

Closing MiNaPAD 2026 Conference by Valérie VOLANT (Auditorium)

Address:

Maison MINATEC
3 parvis Louis Néel
38000 Grenoble

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List of Exhibitors

Booth number	Company
1	CEA
2	ELECTRON MEC
3	MST
4	MICRONOR
5	DYCONEX
6	FINETECH
7	KYOCERA
8	SET
9	SERMA
10	INPACK
11	AEMTEC
12	METRONELEC
13	ACCELONIX
14	ROARTIS
15	ONTOS
16	CICOR
17	SYNERGIE CAD
18	BIESTERFELD
19	ELEMCA
20	CDS
21	HEF
22	UNITEMP
23	PROTAVIC
24	TAIPRO
25	AMADYNE
26	PLASMATREAT
27	HYBRID SA
28	EGIDE
29	CCI EUROLAM
30	GS SWISS
31	INTRASPEC
32	DISCO
33	ELEMATEC
34	ACB
35	ASE
36	INSIDIX

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By Post: IMAPS, 17 rue de l'Amiral Hamelin, 75016 Paris

By Internet: <https://event.imaps.france.org>

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